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Performance Parameter Evaluation of 7nm FinFET by Tuning Metal Work Function and High K Dielectrics

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ABSTRACT

The scrambling of MOSFET below 22nm, 14nm, unwanted Short Channel Effects (SCE) like punch through, drain-induced barrier lowering (DIBL), along with huge leakage current are flowing through the device, which is not recognized for better performance. Multi-gate MOSFET generally measured as Fin-FET is the best substitute vital to stunned short channel effects. The work highlights results of the current-voltage electrical characteristics of the n-channel triple gate Fin-FET gatherings. The paper focuses on the study of geometry-based device design of Fin-FET by changing high k dielectrics materials from silicon SiO2 (3.9), Hafnium Oxide (HfO2), and metal gate work function ranging from 4.1eV to 4.5eV. The approach and simulation of 3Dimensional Fin-FET is carried to evaluate the better performance parameters of device for change in gate length by deploying different dielectrics materials. The effect on ratio of on current (ION) and off current (IOFF), threshold voltage (VTH), subthreshold slope (SS), and drain-induced barrier lowering (DIBL) is observed.

KEYWORDS

DIBL, Dielectrics, FINFET, Fin-FET, Off Current, On Current, SLOPE, SS

INTRODUCTION

CMOS skill is the most fundamental and talented technology in relations of sizing, speed, active power dissipation, high performance & device & circuit level working, etc. The nonstop scrambling in MOSFET length has focused to several challenges that is disappearing gate control on the channel station that marks in Short Channel Effects (SCEs) and heavy leak current. By minimizing the size of the planar transistor i.e. MOSFET below 22nm, several unsolicited effects are occurring like Punch through, subthreshold slope & leakage current. Due to such heavy SCE over nanometer regime, gate is unable to control the channel in the semiconductor(Anju, 2016). To overcome the SCEs, innovative device designs had expected. Multi-gate MOSFET generally considered as Fin-FET which has exposed better downscaling features and improve the performance in terms of speed & low power consumption when related to the MOSFET constructions, due to better gate controllability over the channel.

Fin-FET innovation has been conceived because of the expansion in the degrees of integration. The overview on novelty upgradation activate from vacuum tubes, Point contact diode, BJT, FET, JFET, MOSFET, DG-MOSFET, TG-MOSFET. The gates wound around the channel from the front, top & back sides in Fin-FETs structure, thus the successful diffusion of carriers toward the gate from

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