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Modeling of 7 Nano Meter Fin Field Effect Transistor for Evaluation of Fringe & Oxide Capacitance

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Abstract

Fin-FET are insusceptible to short channel effects punch through, threshold voltage, leakage current but their concerts at high frequencies are conceded due to durable fringing field between gate and source with drain area. Because of high-technology progression, the gate construction of MOSFET has been upgraded from planar to nonplanar with an enrichment in the number of monitoring gates multiple gates on 3 sides. In this paper we mention Fin-FET assembly for high frequency applications.

MOS-FET plays very energetic role but scaling of device affected on performance parameters like speed and power. Fin-FET is non planar novel device to solve the short channel effects which occurs due to scaling. Non-planar structure of Fin-FET parasitic capacitances like gate oxide overlap and fringe capacitance makes adverse effect like lower switching speed of device, making result on delay ion and ioff of device. In this paper we planned Fin-FET design procedure to measure oxide and fringe capacitance with low k dielectric spacer thickness and increase ion to recover device driving ability. Effect on threshold voltage having observed with low k spacer at least count of 0.051 V. By using 4.65 eV metal gate work function with front, top and back gate we control leakage current and threshold voltage. Seven nano meter gate length Fin-FET is design We measured oxide capacitance of 0.464 F for 19.28 GHz and fringe capacitance (69.66 nf) for 4.88 GHz frequency by designing the Fin-FET with high-K SOI MOSFETs which support 11.4 nA leakage current to improve the speed of the processor.

In this research work, design topologies of Single Finger Fin Filed Effect Transistors are discussed and evaluate the probable result of fringe and parasitic capacitance from fringing area on the device. By using geometry of device like fin width, height, thickness and multiple fingers we measure the fringe capacitance and oxide capacitance of designed Fin-FET.

Keywords: CMOS technology, Fin-FET, Parasitic, Thickness, Geometry, Dielectric

Introduction

As per the Moore's law, the degree of transistors in CMOS application are double for each 18 months, in study the scaling of the devices has been done to site a high number of transistors on the chip. Flat transistors structure has unwanted effects like mobility degradation, gate tunneling, giant leakage currents. From former data, as transistor size shrink up to 22 to 10 nm. Double-gate MOSFET is outstanding device for controlling focus of VLSI study since, it can be scaled to the direct channel dimension likely for a specified gate width. Due to double gate structure of MOSFET, the problem of misalignment of top or bottom and front or posterior gate occurs. Fin-FET is one of the innovative approaches having better performance characteristics such as Low leakage current, upgraded short-channel effect.

Multiple fingers are used in Fin-FET, fingers of Fin-FET needed to be stripper due to which sprinkling of dopants increases. We design the triple gate rectangular Fin-FET (TG-Fin-FET. Due to small thickness of fins, the drain current is concentrated as the movement of charge carriers by reducing on current, so to growth the drain current, the quantity of fins has to be improved. **Figure 1** shows the planar horizontally aligned MOSFET structure which contain gate drain and source. **Figure 2** shows Non planar vertically aligned Fin-FET model which contains 3 gates on front, back and top side with drain and source terminal.