"Device Design of 30 and 10 nm Triple Gate Single Finger Fin-FET for on Current (I_{ON}) and off Current (I_{OFF}) Measurement"

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Abstract Nowadays, users need portable gadgets like laptops and cellular phones with small in size which occupies less area, consumes low power and having low cost. Justifying Moore's law by designing the smaller size transistors on the silicon wafer, more numbers of transistors available on a single wafer help to design complicated circuits with very low cost. Scaling plays vital role to decide the size of transistor with high performance. Most attracted multi-gate technology for researchers as well for industry is Fin-FET for nano-scale design. The nano-scale Fin-FET technology provides best solution for Moore's law. This paper focuses on how Fin-FET helps to reduce short channel effect and also presents design of 30 nm and 10 nm single Fin-FET with Triple Gate. Leakage current, threshold voltage and drain drive current evaluated from device design by using high K of dielectric material. Simulation carried out using COMSOL MULTIPHYSICS Version 5.3

1 Introduction

Scaling has been expected toward smaller size, advanced speed, low stimulus and higher density of the semiconductor devices. As MOSFET channel thickness is climbed to the nano-meter regime, the gate cannot handle the position activity so damage the control action on the channel, and some critical belongings are occurred like hot carrier things, punch through, mobility degradation and short channel properties are occurring.

CMOS skill introduces the size of the device reduced to 10 micrometer in 1971 near 90 nanometer, and now in 2020 we avoid thesepossibly, we will shrink the to below 10 nm (7 nm, 5 nm). Size reductions of transistor cause unwanted technological effect that is short channel effect. Existing CMOS technology has a big problem of

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