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SURFACES, INTERFACES, AND THIN FILMS

Bulk Fin-FET Strategy at Distinct Nanometer Regime for Measurement of Short-Channel Effects

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Abstract—The planar structure of MOSFET invites uncertainties that can't reduce the short-channel effects (SCE) like drain-induced barrier lowering (DIBL), punch through, and sub-threshold slope (SS). Fin-FET technology can be a better choice. It is a technology that uses more than one gate, called multiple gate devices, which is an improved technology option for further shrinking the size of the planar MOSFET. In this work, we inspect possibilities of gate-length and fin-thickness scaling in triple-gate single Fin-FET device design to solve the problem of SCE and progress the performance of the nanoscale device. The electrical characteristic parameters of the nanoscale device like threshold voltage, SS, DIBL, and leakage current are evaluated from DC characteristics (transfer and output) by proposed design. The findings offer the drain-induced barrier lowering, threshold voltage, and leakage current by calculation. From the simulation results, we observe lowering of DIBL, SS, and leakage current, whereas threshold voltages rise. A triple-gate N-Fin-FET is designed with different fin thickness and gate length in scaling with 14, 10, and 7 nm, and the effects are observed on the improved performance of the device. 3D Single Fin-FET structure is designed successfully, and we plot the current–voltage *I–V* output and transfer characteristics.

Keywords: SCE, modeling, BSIM-CMG, ITRS, DIBL, threshold voltage

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1. INTRODUCTION

In divergence to the planar CMOS, Fin-FET can have only widths that are multiple to a value, since the required width is obtained by placing several fins in parallel. The current drive capability of multiple-gate MOSFET is proportional to total gate width. Fin-FET has double-gate (DG) and triple-gate (TG) structure with lower control of Fin thickness as shown in Figs. 1 and 2.

Triple-gate Fin-FET is a thin film narrow silicon island, and provides symmetric device architecture where the channel length is measured by the gate from three sides of the silicon (Si) film. So, gate control increases. The operational difference between TG and DG is that in DG Fin-FET the gate oxide layer is denser at the top part of the fin so that only two gates remain effective for the channel (front and back), while in TG the channel is formed on the top surface as well as side surface, and this will increase the areal density of On-current. As shown in Fig. 1, the gates are connected electrically, i.e., they are shorted gates.

In insulated gate Fin-FET, two gates are not electrically connected.

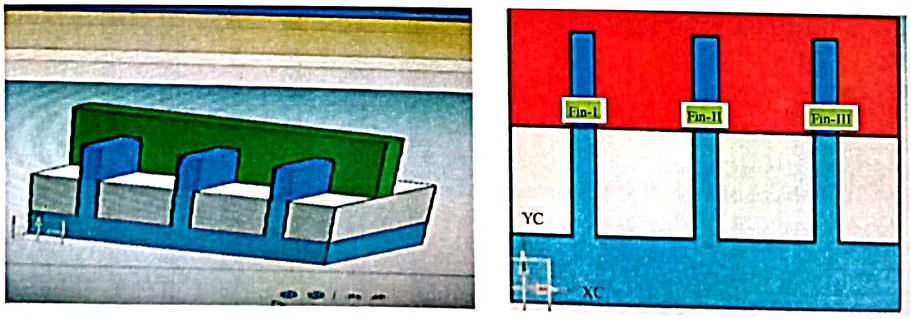

Fig. 1. Fin-FET construction.