

# Design Issues & Challenges with EMI/EMC in System on Packages (SOPs)

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**Abstract-**Every electronic product has been subjected to EMC/EMI regulations by several international bodies such as FCC, IEC; if the frequency of operation exceeded 9Khz. The interference generated by electronic gadgets was easily manageable in earlier years. As the complexity and speed of circuits increased, intersystem and intrasystem interference gained prominence. The factors such as closely placed conductors, greater number of vias which allow the gadgets become more compact and hence become the inherent source of electromagnetic radiations affecting other devices /circuits on SOP, disregarding them may prove costly in the later stage of the design flow. In today's SOPs, high performance digital LSIs are sources of EMI, while RF and analog circuits are affected by EMI. In future, electronic systems shall require higher bandwidth with lower power consumption to handle massive amount of data, especially for large memory systems, high-definition displays, and high-performance microprocessors, and not only this noise margins shall also reduce due to reductions in power supply voltages, and hence noise voltages generated due to EMI may be comparable to shrunk noise margins, ignoring them may cause the system to malfunction.

**Index terms-**RPDs,EMI,SOP,Vias,Cavity Resonance, Power planes.

## I. INTRODUCTION

Printed circuit boards (PC Boards) have been the part and parcel of every electronic circuits and equipments. Until 1980 the PCBs used to operate at frequencies limited to few MHz .The advent of fast computers and their fast processors increased the speed of signals in motherboard of computers. The growing popularity of mixed integration has created significant PCB design challenges to suppress high-frequency electromagnetic interference.

EMI in System On Chip (SOP): The factors responsible for electromagnetic interference (EMI) mechanism in real electronic products are LSI design, package structure design, printed circuit board (PCB) wiring design and enclosure design. The signal transmission from one chip to another on an SOP can excite two types of noise sources, i) normal mode type radiation due to the signal-return path loop ii)common mode excitation of the power/ground plane due to switching currents from LSI.When excited by switching currents, the power/ground plane can act as an unwanted antenna at the resonant frequencies.

## II OVERVIEW OF EMC

A. History: In the early years (i.e. before 1990s) the Clock frequencies below 25 MHz EMI/EMC design was not done in early stages of product development, the late identification of problems, hence delay in product release.

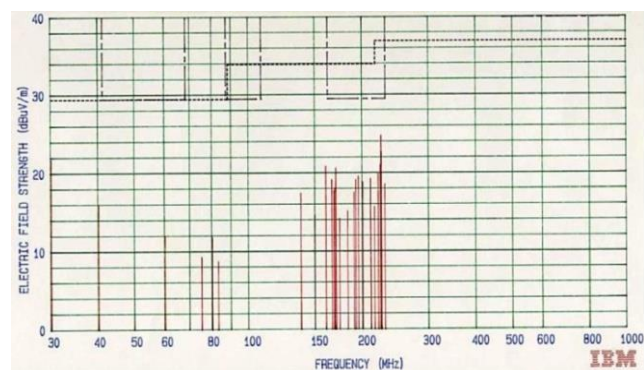


Fig.1 EMC plot in 80s [13]

In the nineties, the CPU Speeds exceeded 1GHz.The EMI/EMC design was done in early stages of product development. Emissions became more pronounced as wavelengths have become comparable to devices mostly from devices & interconnects .

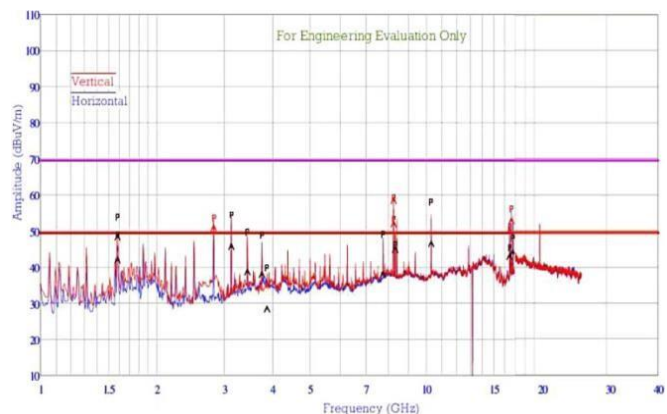


Fig.2 EMC plot 2009 onwards [13]

B. Generation Of EMI in SOPs